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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/713,753	
	Filing Date	November 13, 2003	
	First Named Inventor	Bruce W. MCGAUGHY	
	Art Unit	2123	
	Examiner Name	A. Pierre-Louis	
Total Number of Pages in This Submission	5	Attorney Docket Number	188122002000

ENCLOSURES (Check all that apply)

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Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	MORRISON & FOERSTER LLP (Customer No. 25226)		
Signature			
Printed name	Thomas Chan		
Date	June 15, 2007	Reg. No.	51,543

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Docket No.: 188122002000
Client Ref. No.: CAD: 03-094
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Bruce W. MCGAUGHY et al.

Application No.: 10/713,753

Confirmation No.: 1627

Filed: November 13, 2003

Art Unit: 2123

For: SYSTEM AND METHOD FOR SUPPORTING
MULTI-RATE SIMULATION OF A CIRCUIT
HAVING HIERARCHICAL DATA
STRUCTURE

Examiner: A. Pierre-Louis

COMMUNICATION UNDER 37 C.F.R. 1.97(i)

MS Issue Fee
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Alexandria, VA 22313-1450

Dear Sir:

Applicant respectfully requests that the attached reference be placed in the file wrapper for the above-referenced application, in accordance with the provisions of 37 CFR 1.97(i).

Applicant certifies that none of the references submitted herewith was first cited in any communication from a foreign patent office in a counterpart foreign application or, to the best of Applicant's knowledge after making a reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c), more than three months prior to the submission of this communication.

Applicants believe no fee is necessary but in the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of

such petitions and/or other fees due in connection with the filing of this document to Deposit
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Dated: June 15, 2007

Respectfully submitted,

By 

Thomas Chan

Registration No.: 51,543

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ALTERNATIVE TO PTO/SB/08A/B (04/07)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/713,753
				Filing Date	November 13, 2003
				First Named Inventor	Bruce W. MCGAUGHY
				Art Unit	2123
				Examiner Name	A. Pierre-Louise
Sheet	1	of	1	Attorney Docket Number	188122002000

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1.	Chakrabarti, D.R. et al. (November 23-24, 1995). "An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-circuits," <i>Proceedings of the Fourth Asian Test Symposium 1995</i> , 1:237-243.	
	2.	Jones, L.G. et al. (February 1994). "A Cache-Based Method for Accelerating Switch-Level Simulation," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> 13(2):211-218.	
	3.	Smith, III, J.O. (August 26, 2006). "Radix 2 FFT Complexity is N Log N," <i>In Mathematics of the Discrete Fourier Transform (DFT), with Music and Audio Application</i> , W3K Publishing: Stanford, located at < http://ccrma.stanford.edu/~jos/mdft/Radix_2_FFT_Complexity.html >, last visited on October 19, 2006, 1 page.	
	4.	Wong, Y. (1985). "Hierarchical Circuit Verification," <i>IEEE 22nd Design Automation Conference</i> , pp. 695-701.	

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